AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-3 (canceled).

Claim 4 (currently amended): A register circuit ~~according to claim 2,~~ having a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and providing an output data,

said clock signal being a charge recycled clock signal having a gradually rising and gradually falling non-rectangular waveform generated by using a charge recycle power source in which power supplied to a load is at least partially collected and returned to said charge recycle power source, and

the following inequality is satisfied:

$|V_{TN}| + |V_{TP}| \geq VDD$

where V_{TN} is a threshold of said n-channel MOSFET transistor, V_{TP} is a threshold of said p-channel MOSFET, and VDD is an output voltage of said charge recycle power source,

wherein said register circuit comprises a pair of D-latch circuits with an input of a

second D-latch circuit coupled with an output of a first D-latch circuit, a first D-latch circuit accepts a first power clock signal, and a second D-latch circuit accepts a second power clock signal which is different by 180° phase of the first power clock signal, and

wherein said register circuit includes a combination logic circuit between said pair of D-latch circuits.

Claim 5 (canceled).